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On APRIL 9, 2003
By: /Karen A Hallock/
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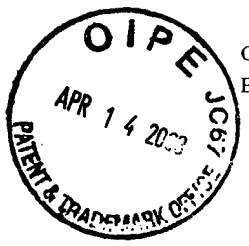
Attorney Docket No.: ONCHP001



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

BULENT DERVISOGLU et al.

Application No.: 09/275,726

Filed: March 24, 1999

For: ON-CHIP SERVICE PROCESSOR FOR TEST AND DEBUG OF INTEGRATED CIRCUITS

Examiner: D. TON

Art Unit: 2133

SUPPLEMENTAL APPEAL BRIEF

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Sir:

Real Party in Interest

The real party in interest is On-Chip Technologies, Inc., the assignee of the present patent application and wholly owned corporation of the applicant/inventors.

Related Appeals and Interferences

There are no interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

An appeal was taken from the final Office Action of October 31, 2001 with an Appeal Brief filed April 24, 2002. Prosecution was reopened by a subsequent Office Action of February 6, 2003, which withdrew the final Office Action and set forth new grounds of rejection. This Supplemental Appeal Brief supports the accompanying Request for Reinstatement of Appeal taken from the February 6, 2003 Office Action and is filed pursuant to 37 CFR §1.193(b)(2)(ii).

Status of Claims

All claims 1-22 are pending; all claims 1-22 are appealed.

Status of Amendments

No amendments have been filed subsequent to the rejection of all claims 1-22 in the final Office Action of October 31, 2001, nor subsequent to the Office Action of February 6, 2002.

Summary of Invention

The present invention is related to the internal testing and debugging of an integrated circuit, as compared to the testing of an integrated circuit externally or as part of a larger electronic system. Generally stated, there are two ways of testing and debugging an integrated circuit internally, both of which are described in the applicants' specification. One way is to serially "scan" test vectors, sets of predetermined bits, into predetermined locations in the integrated circuit, operate the integrated circuit for one or more clock cycles, and then scan out the test results from the locations in the integrated circuit. See applicants' specification, page 2, lines 4-33. The other way is to "probe" the integrated circuit, that is, to observe the internal workings of the integrated circuit in its normal operation, i.e., *in situ*. See, for example, applicants' specification, page 3, lines 1-15. The applicants' present invention, as reflected by the pending claims under appeal, is directed toward the latter probing technique.

The device aspects of the present invention are reflected in independent claims 1 and 10. In one aspect of the applicants' invention, the integrated circuit has a control unit, a memory and a plurality of probe lines. The control unit performs test and debug operations on the logic blocks of the integrated circuit. The memory, which is associated with the control unit, holds instructions for the control unit and stores the system operation signals from the logic blocks. Responsive to the control unit, the probe lines carry the system operation signals from predetermined probe points of the logic blocks to the memory for storage. The probe lines comprise strings of storage elements which provide the signal paths from the probe points to the memory to move sets of the system operation signals at system operation clock rates. See applicants' specification,

page 7, lines 9-21; page 17, lines 9-27; Fig. 11. In other words, the internal clock(s) of the integrated circuit are used to move the system operation signals at high speed into the memory. The sets of system operation signals are stored in the memory for subsequent retrieval and analysis. Applicants' specification, page 6, lines 20-30.

Another device aspect of the invention is that the integrated circuit has an interface for coupling to an external diagnostic processor. Applicants' specification, page 16, lines 15-20; page 17, lines 21-22; and Fig. 1b. The control unit is responsive to instructions from the external diagnostic processor to capture sets of sequential system operation signals of the integrated circuit through the probe lines into the memory. The memory is coupled to the control unit and the interface so that the stored sets of sequential system operation signals are retrieved from the memory through the interface to the external process at one or more clock signal rates external to the integrated circuit so that the external diagnostics processor can process the captured system operation signals for analysis. Applicants' specification, page 19, lines 8-21.

Still another aspect of the present invention is related to the operation of the integrated circuit and reflected in independent method claim 15. The following steps are used: operating the logic blocks of the integrated circuit to perform normal system operations at the integrated circuit's normal clock rates to produce *in situ* sets of system operation signals, i.e., the normal system operation signals; enabling probe lines in the integrated circuit to capture and carry the sets of the system operation signals of the logic blocks at the normal clock rates; retrieving the sets of system operation signals from the logic blocks along the probe lines at the normal clock rates, storing the sets of the system operation signals in a memory in the integrated circuit at the normal clock rates; and processing the sets of stored system operation signals to perform test and debug operations of the logic blocks of the integrated circuit. The applicants' specification at page 19, lines 8-21, has a description of such probe testing with an external diagnostic console.

Issues

Only one basic issue is appealed, that is, whether the Examiner has made a proper case of obviousness in rejecting the applicants' invention as recited in independent

claims 1, 10 and 15. The applicants argue below that the Examiner has not even met the criteria for a *prima facie* case. All of the independent claims are allowable and since the independent claims are allowable, all remaining claims 2-9, 11-14, and 16-22 are also allowable. That is, all pending claims 1-22 should be allowed and passed to issue.

Grouping of Claims

Claims 1-10 and 13-22 were rejected for obviousness by the combination of the Whetsel and Gheewala '090 patents, U.S. Patent Nos. 6,131,171 and 5,065,090 respectively. The claims of this group do not stand nor fall together, rather independent claims 1, 10 and 15 are separately patentable. See the description above in the Summary of the Invention.

Dependent claims 11-12 were also rejected for obviousness by the combination of the Whetsel and Gheewala '090 patents, and a second Gheewala patent, U.S. Patent No. 5,202,624. The applicants do not select a representative claim for this group since the rejection of the previous claim grouping presents more significant issues for appeal.

Argument

Applicants' claims 1-10 and 13-22, including independent claims 1, 10 and 15, were rejected under 35 U.S.C. §103(a) for obviousness over the combination of U.S. Patent No. 6,131,171, which issued October 20, 2000 to L.D. Whetsel (hereinafter the "Whetsel patent"), in view of U.S. Patent No. 5,065,090 which issued November 12, 1991 to T. Gheewala *et al.* (hereinafter the "Gheewala '090 patent").

The Whetzel patent upon which the Examiner primarily relies teaches a technique "for observing data on a bus connecting multiple integrated circuits," as stated in the Technical Field of the Invention of the Whetsel specification, because "the ability to dynamically observe digital **signals on buses** formed on leads on the substrate or circuit board **between integrated circuits** has been unavailable (emphasis added)." Col. 1, lines 41-43. The Whetzel patent is not directed toward the testing and debugging of the internal workings of an integrated circuit, but rather the interconnections (more specifically, the bus connections) between integrated circuits on a circuit board. The disclosed digital bus monitor (DBM) circuits are connected to the buses between

integrated circuits on the circuit board for purposes of "production testing to field service and maintenance" of the circuit boards. Whetsel patent, col. 2, line 20.

The secondary Gheewala '090 patent, on the other hand, is directed toward the testing of the internal integrity of an integrated circuit; a particular serial scan testing circuit and technique is taught in the patent. In serial scan testing, the integrated circuit to be tested is placed in a test operation (as opposed to normal operation) mode, and test pattern signals, sometimes called a test vector, are scanned into the integrated circuit at selected locations to place those selected locations in the integrated circuit into known states. The resulting test response data, sometimes termed test results, are scanned out for analysis. To perform this serial scan testing, the Gheewala '090 integrated circuit has a grid test structure with intersecting probe lines P1-PN (despite the similarity of terminology to applicants' claims, Gheewala's probe lines carry control signals, as opposed to system operation signals) and sense lines S1-SM (carrying signals to or from the integrated circuit sense points). See Gheewala '090 patent; Fig. 4. At each intersection, an electronic switch responsive to a control signal on a probe line controls the connection of a sense point to a sense line. A serial/parallel shift register 27 is connected to the probe lines P1-PN and a second serial/parallel shift register 28 is connected to the sense lines S1-SM to provide on-chip test electronics to reduce the number of probe points, i.e., test pins, for the integrated circuit, a goal of Gheewala patent. See, for example, the Abstract of the Gheewala '090 patent; Fig. 4 and col. 8, lines 21-56 of the specification.

The applicants argue below that the Examiner's rejections of independent claims 1, 10 and 15 do not even meet a *prima facie* case for obviousness, which under MPEP §2143 requires:

> "...First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. Second, there must be reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

None of these requirements are met.

I. THERE IS NO SUGGESTION NOR MOTIVATION TO MAKE THE COMBINATION OF THE WHETSEL AND GHEEWALA '090 PATENT REFERENCES.

Except for the identification of an additional element in the Whetsel patent as an analog to one of applicants' claimed elements, the Examiner's basis for rejecting device claim 10 is identical to that of device claim 1, and the reasoning for rejecting method claim 15 is also based on the same references combined in the same way. Hence the applicants' arguments with respect to claim 1 are also applicable to claims 10 and 15.

Applicants' claim 1 calls for:

> "An integrated circuit having logic blocks comprising
> a control unit for performing test and debug operations of said logic blocks of said integrated circuit;
> a memory associated with said control unit, said memory holding instructions for said control unit; and
> a plurality of probe lines responsive to said control unit for carrying system operation signals from predetermined probe points of said logic blocks, wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said memory, said signal paths capable of moving sets of said system operation signals at system operation clock rates, said sets of system operation signals stored in said memory so that said sets of system operation signals are retrievable."

In rejecting claim 1, the Examiner stated:

> "Whetsel teaches the invention as substantially as claimed [see claim 1], including an integrated circuit IC 10 of Fig. 1] having logic blocks [see Fig. 2] comprising:
> "a control unit [TCR control 26 of Fig. 2] for performing test and debug operations of said logic blocks of said integrated circuit [see claim 1];
> "a memory [memory 30 of Fig. 2] associated with said control unit, said memory holding instructions for said control unit.
> "Whetsel teaches a plurality of probe lines [ODI of Fig.1&2] coupled to said control unit for carrying said system operation signals from predetermined points [data bus 16 of Fig. 1] of said integrated circuit to said memory [DBM of Fig. 1], wherein said lines providing signal paths from said point to said memory, said signal path capable of moving sets of said system operation signals at system operation clock rates, said sets of system operation signal stored in said memory so that said sets of system operation signal are retrievable [see col. 4 lines 41-68 and claim 1].

> However, Whetsel does not explicitly teach the plurality of probe lines comprises strings of storage elements for carrying said system operation signals.
>
> "Gheewala teaches a cross-check test structure consists of serial/parallel shift registers with probe lines and sense lines to control the probe lines and to observe the output of the sense lines [Fig. 4 and col. 8 lines 21-56].
>
> "It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the ODI of Whetsel to include the probe lines comprising a string of storage elements as taught by Gheewala for carrying data signals from the data bus to the memory. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so as a matter of design choice by the events detected over a range of DBM devices [see Whetsel col. 4 lines 54 – col. 5 line 13]." Paragraph 7, pages 3-4 of the outstanding Office Action.

The Examiner's combination is the system illustrated in the Whetsel's Fig. 1 with Gheewala's "serial/parallel shift registers with probe lines and sense lines to control the probe lines and to observe the output of the sense lines" inserted into, or in place of, the ODI lines connecting the address and data buses 14 and 16 with the DBM1 20 and DBM2 22 integrated circuits.

With due respect to the Examiner, the combination is artificial and forced. There is no suggestion nor motivation to make the combination of cited references as suggested by the Examiner for at least three reasons. The first is that the motivation which the Examiner asserts is simply not related to the purported combination; the Examiner's "motivation" does not even lead to the combination. The second is that the arbitrariness of the combination of the Whetsel system and the Gheewala serial/parallel shift registers negates any suggestion to make such a combination. Finally, the suggested combination results in a crippled version of the Whetsel system; rather, one skilled in the art would avoid the combination.

First, the Examiner asserts that the motivation for making his combination is because "a person having ordinary skill in the art would have been motivated to do so as a matter of design choice by the events detected over a range of DBM devices [see Whetsel col. 4 lines 54 – col. 5 line 13]." This "motivation" is simply fanciful. The detection of events over a range of DBM devices is unrelated to the insertion or

substitution of serial/parallel shift registers for the ODI lines in the purported combination.

The Whetsel patent itself teaches how to handle events detected over a range of DBM devices. As explained in col. 4, lines 41-53 of Whetsel, the DBMs 20 and 22 can monitor on-line the data and address buses 14 and 16 connecting the two integrated circuits 10 and 12 with EQMs (Event Qualifying Modules) 32 located in each DBM. With comparator circuitry, the EQMs 32 issue control signals to capture the data on the ODI lines when the data appearing the ODI lines match certain known or expected data patterns, i.e., events. The sections of the Whetsel patent cited by the Examiner describe the connection of more EQMs 32 (in the DBMs) "to expand event qualifying capability." Col. 4, line 54. Specifically, "...multiple DBMs (or other devices containing the EQM and the EQI and EQO pins) can be connected together on an external combining network 24, such as AND gate 24, to allow the qualification of a test monitor operation to be controlled by the events detected over a range of DBM devices." Col. 4, lines 54-59. Whetsel suggests the addition of more DBMs (with their EQMs) connected to the buses by ODI lines in parallel with the two DBMs 20 and 22 to monitor events on the buses 14, 16 and 18, in the Fig. 1 system. The EQOs (Event Qualifying Outputs) of the added DBMs are connected as additional inputs to the AND gate 24.

It is unclear how the insertion into, or replacement of, the ODI lines by Gheewala's serial/parallel shift registers enhances the test monitor operation controlled by events over a range of DBM devices. This relationship between Gheewala's serial/parallel shift registers and the Whetsel's test monitoring controlled by the events over a range of DBM devices is not explained and, the applicants assert, is inexplicable because the two are unrelated. The asserted motivation for the combination is a simple contrivance to make the applicants' claims.

Secondly, the arbitrariness of the combined elements reflects the artificiality of any motivation for the combination. The Whetsel Fig. 1 system provides nearly of all the elements of the combination. To make the applicants' claims, only one element of one embodiment of the Gheewala '090 patent is added. In place of, or into, the ODI lines which connect the buses between integrated circuits to the DBM (Digital

Bus Monitor) integrated circuits in the Whetsel Fig. 1 system, the Examiner places serial/parallel shift registers from Fig. 4 of the Gheewala patent. On the one hand, the Whetsel patent is directed toward the testing of circuit boards and the integrated circuits mounted on the boards. The Gheewala '090 patent, on the other hand, is directed toward the serial scan testing of an integrated circuit, which, in turn, is different from the probe techniques claimed by the applicants. See the Summary of the Invention and the applicants' description above of the Gheewala '090 patent. In particular, the purpose of Gheewala's serial/parallel shift registers is to reduce the number of probe points, i.e., pins, to implement his cross-check test technique, see col. 8, lines 57-59, a purpose unrelated to the Examiner's suggested "motivation" or to Whetsel's system. There is no reason to make the particular combination urged by the Examiner.

Thirdly, there is motivation **not** to make the suggested combination. As pointed out below in Section II., the combination is flawed, i.e., the combination adversely affects the performance of the Whetsel system and adds needless complexity without attendant gains in functionality.

Hence the asserted motivation to make the combination of references is a contrivance. There is no relationship between the asserted motivation to make the combination and the resulting combination. The combination of the Whetsel system elements and the Gheewala serial/parallel shift registers is arbitrary; the purposes of the Whetsel and Gheewala patents and their elements are unrelated to each other. There is no reason to make the combination suggested by the Examiner. Finally, one skilled in the art would be motivated not to make the combination since the suggested combination at best has no advantages over Whetsel's original system, as shown immediately below.

II. THE COMBINATION OF THE WHETSEL AND GHEEWALA '090 PATENT REFERENCES HAS NO EXPECTATION OF SUCCESS.

To reject applicants' independent claims 1, 10 and 15, the same combination of the Whetsel patent with the Gheewala '090 patent was used. Accordingly the applicants make a single argument with respect to claim 1 as representative for all the independent claims. Specifically, the Gheewala '090 patent was characterized as teaching "...a cross-check test structure consists of serial/parallel shift registers with probe lines

and sense lines to control the probe lines and to observe the output of the sense lines [Fig. 4 and col. 8 lines 21-56], " and the combination is "to include the probe lines comprising a string of storage elements as taught by Gheewala for carrying data signal from the data bus to the memory." Office Action, pages 3-4. However, the Examiner did not give the details of the substitution or insertion of the Gheewala serial/parallel shift registers for or into, the ODI lines of the Whetsel system. There are two possibilities; neither of which leads to a combined system with any expectation of success.

The most likely possibility is the insertion of a Gheewala serial/parallel shift register into the ODI lines similar to the arrangement of the shift register 28 described with respect to Gheewala Fig. 4. A serial/parallel shift register is laid across the plurality (16 in Whetsel's specific embodiment, see col. 7, line 13) of ODI lines so that the shift register can capture the signal bits on the ODI lines in parallel mode and then shift them out in serial mode in accordance to the Gheewala operation described as follows. "The signals present on the sense-line (S1-SM) are next stored in shift register 28 connected to the sense lines. This is achieved by applying an external control signal to the parallel/serial control 29 to put the shift-register 28 in the parallel mode and turning the clock 30 ON once. The signals on the sense-lines are now stored in the sense shift-registers 28. Next, the signals stored in the shift-register 28 can be serially read out at probe-point 32 for analysis by external test electronics. This is achieved by applying an external signal to the parallel/serial control probe-point 29 to put the shift-register 28 in a serial mode and turning the clock 30 ON and OFF M times (parenthetical expression added)." Col. 8, lines 33-45. The serial/parallel shift register 28 carries signals sensed in the integrated circuit system.

A more remote possibility is the insertion or substitution of a shift register into each ODI line similar to the arrangement of the shift register 27 of Gheewala's Fig. 4. "The outputs of the shift–register 27 control the probe–lines P1 through PN and are designed to activate only one probe-line at a time during testing. When a specific probe-line is activated, the electronic signals on the test-points connected to the switches controlled by that specific probe-line are transferred to the sense lines S1 through SM." Col. 8, lines 27-33. "Similarly, the control data on the probe-line shift-register 27 can be

loaded from external test electronics in by presenting the data in a serial manner at the input probe-point 33 and by turning the clock 34 ON and OFF N times." Col. 8, lines 45-49. The net result is that each of the (16) ODI lines of Whetsel is replaced by an N-stage shift register. This arrangement is more remote because this use of serial/parallel shift registers in the combination are further removed from the teachings of Gheewala. The shift register 27 taught by Gheewala, does not carry test result signals for storage and analysis, but rather control signals to perform the test operation. Additionally, one of the functions of the shift-register 27 in the Gheewala patent, the parallel output for control, has been arbitrarily eliminated so that the function of the shift-register 27 has been changed. There is no teaching in the Whetsel nor Gheewala patent to do so.

In any case, neither arrangement is successful. In the first arrangement, what arrived over the parallel ODI lines in one clock cycle of the Whetsel system of Figs. 1 and 2 must now travel serially over the inserted serial/parallel shift register 28. If M = 16, then there must be at least 16 clock cycles before the ODI data is available to the Whetsel system. The Whetsel system must now operate at $1/16^{th}$ of its former speed; the system has been slowed to a crawl. Such a speed retardation must surely destroy the ability to observe the bus data between the integrated circuits 10 and 12 as they operate and vitiates the purpose of Whetsel's invention. See, for example, col. 2, lines 1-4.

In the second arrangement, the data on the ODI lines must travel serially over the N-stage shift registers before reaching the DBMs 20 and 22. Hence operations are now delayed for N clock cycles for some unknown reason. This assumes that the external clock signals are free-running. If the clock signals are not free-running, i.e., the clocks only operate on valid data sequences on the ODI lines, the information on the N-stage shift registers may not be observed before the next the test is invoked. The point here is that a needless complication has been introduced by this arrangement.

Hence the Examiner's purported combination of the Whetsel and Gheewala '090 patents yields a failed system. In one arrangement the resulting system must operate much more slowly and subverts the purpose of the original Whetsel system. In the second arrangement, the combined system operates with a time delay at best and is needlessly complex at worst. No advantage for such a system is manifest. The addition

of circuitry to a functioning system with no benefits, as suggested by the Examiner, is abhorrent to common engineering economy. Furthermore, neither arrangement makes sense in view of the purported reason for the combination of references, i.e., "because it would enhance the test monitor operation to be controlled by the events detected over a range of DBM devices...". In fact, there is no reason for the combination.

Hence, viewed in the best light, the suggested combination is a poor version of the original Whetsel circuit board testing system; the combination is an electronic version of a Rube Goldberg contraption which thrashes about with nominal benefits.

III. THE COMBINATION OF THE WHETSEL AND GHEEWALA '090 PATENTS DOES NOT EVEN MEET THE LIMITATIONS OF APPLICANTS' CLAIMS.

As argued out above, the combination of the Whetsel and Gheewala '090 patents as suggested by the Examiner, is artificial and forced. Furthermore, the combination does not even meet all the limitations of independent claims 1, 10 and 15, as shown below.

A. The Combination of Cited References Does Not Make the Limitations of Claim 1.

For reading convenience, applicants' claim 1 is again reproduced:

> "An integrated circuit having logic blocks comprising
> a control unit for performing test and debug operations of said logic blocks of said integrated circuit;
> a memory associated with said control unit, said memory holding instructions for said control unit; and
> a plurality of probe lines responsive to said control unit for carrying system operation signals from predetermined probe points of said logic blocks, wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said memory, said signal paths capable of moving sets of said system operation signals at system operation clock rates, said sets of system operation signals stored in said memory so that said sets of system operation signals are retrievable."

Even assuming *arguendo* that the combination of the Whetsel and the Gheewala '090 patents can made, the purported combination simply does not teach nor suggest the limitations of claim 1. The limitations of an 1) "integrated circuit;" 2) "probe

lines responsive to said control unit;" and 3) "memory...holding instructions for said control unit" are not met by the combination, as argued below.

1. The Whetsel System of Integrated Circuits Is Not the Applicants' Claimed "Integrated Circuit."

The applicants' invention is directed toward the testing and debugging of the inner workings of an integrated circuit. See the Summary of the Invention above. Claim 1 recites, "An integrated circuit ... comprising ...," followed by a list of constituent elements which comprise the integrated circuit in accordance with standard patent practice.

In his rejection of claim 1, the Examiner stated, "Whetsel teaches the invention as substantially as claimed [see claim 1], including an integrated circuit IC 10 of Fig. 1] having logic blocks [see Fig. 2] comprising: ...a control unit [TCR control 26 of Fig. 2]...". The basis of the claim 1 rejection is reproduced in its entirety on pages 7-8 of this Supplemental Appeal Brief. This principal reliance of the Whetsel Fig. 1 system is a fundamental misreading of an integrated circuit (applicants' claim 1) as a circuit board testing system with several integrated circuits (Fig. 1 of Whetsel). Obviously, an integrated circuit is not a system of integrated circuits. See Whetsel's description of his Fig. 1 circuit board system at col. 3, lines 38-49, for example.

Additionally, in explaining the basis for this fundamental misreading, the Examiner compounds his error with self-contradictory identification of the applicants' elements in the Whetsel system. The Whetsel patent is directed toward circuit board testing by the monitoring of digital signals carried on bus connections between integrated circuits on a circuit board. IC1 10, the integrated circuit identified as corresponding to the applicants' integrated circuit, is one of the integrated circuits on the circuit board represented by Whetsel's Fig. 1. The applicant's recited "logic blocks" in the preamble of claim 1 are accordingly identified as part of IC1 10 but are also referred to in Fig. 2 of the Whetsel patent. However, Fig. 2 "illustrates a block diagram of the digital bus monitor integrated circuit, (col. 2, lines 49-50 of the Whetsel patent)," i.e., either DBM-1 20 and DBM-2 22 which are connected to the IC1 10 in Fig. 1. In other words, Fig. 2 is the block organization of an integrated circuit which is **not** IC1 10. This is readily

evident by the underlined reference number, "20", in its upper right-hand corner of the dotted rectangle which encompasses most of Fig. 2.

This confusion between the integrated circuits IC1 10 and DBM-1 20 and its constituent elements is constant in the rejection of claim 1. For example, the applicants' "control unit" and "memory" elements are respectively identified as "TCR control 26 of Fig. 2" and "memory 30 of Fig. 2." According to claim 1, these elements should be part of IC1 10. However, TCR control 26 and memory 30 are elements of DBM-1 20, not IC1 10.

The result is that claim 1, which recites an integrated circuit and its constituent elements, is rejected over Whetsel's circuit board system having IC1 10 (supposedly applicants' integrated circuit) and the DBM 20 and 22 integrated circuits illustrated in Fig. 1. The elements of DBM-1 20 pictured in Fig. 2 of the Whetsel patent are misidentified as providing the constituent elements of the applicants' integrated circuit.

But even accepting *arguendo* this fundamental misreading of the Whetsel patent, the elements of the reference identified with the elements of applicants' claim 1 still do not teach the limitations of the claim.

2. The Whetsel System Has No "Probe Lines Responsive to Said Control Unit."

Claim 1 calls for "a control unit for performing test and debug operations of said logic blocks of said integrated circuit..." and "a plurality of probe lines responsive to said control unit for carrying system operation signals from predetermined points of said logic blocks...". The Examiner has analogized the applicants' "control unit" to the TCR control register 26 and the "plurality of probe lines" to the ODI (observability data input) lines which connect the DBM-1 10 and DBM-2 12 (integrated circuit) blocks to the data bus 16 and address bus 14 respectively. See Fig. 1 of the Whetsel patent.

However, the TCR control register 26 does not control the ODI lines to carry digital signals from the buses 14 and 16. Rather, the TCR control register 26 holds signals for the TCR (test cell register) 28 to handle the data on the ODI lines. "The TCR control register 26 is used to store configuration signals that are used to mask off ODI inputs to the TCR 28, select the TCR's polynomial tap configuration and adjust the TCR

28 for cascading with TCRs in other DBM devices." Col. 6, lines 43-46. If anything, the data movement through the ODI lines appear to be controlled by the EQM (event qualification module) 32 in the DMB 20. "During on-line monitoring the internal EQM of each DBM device 20 and 22 outputs control signals to capture the data appearing on the ODI inputs of the respective DBMs." Col. 4, lines 44-47. Of course, given the differences between the Whetsel system and the applicants' claim, analogization of the EQM 32 with the applicants' "control unit," leads to other mismatches between the claim language and the cited reference.

3. There is No "Memory...Holding Instructions for Said Control Unit" In the Whetsel System

The Examiner further identifies the memory 30 in the Whetsel patent as the analog to the applicants' "memory." But claim 1 also calls for "a memory associated with said control unit, said memory holding instructions for said control unit...". Nowhere does the Examiner explain how the memory 30 holds instructions for the identified control unit, the TCR control register 26.

In fact, the memory 30 does not hold instructions for the TCR control register 26, which "receives input from the command bus 44, and control bus 48." Col. 6, lines 47-48. The memory 30 does not download anything, much less instructions, to the TCR control register 26. This is evident from the diagrams and connections shown in Fig. 2. The list of connections for the memory 30, recited in col. 10, lines 19-26, do not mention a connection to the TCR control register 26 and ends in the statement, "The memory 30 outputs a TDO signal." Nowhere is there described how the TDO (Test Data Out) signals lead back to the TCR control register 26 and affect its operation, as a command instruction should.

B. The Combination of Cited References Do Not Make The Limitations Of Claim 10.

Applicants' claim 10 calls for:

> "An integrated circuit comprising
> an interface for coupling to an external diagnostic processor;

a unit responsive to instructions from said external diagnostic processor for capturing sets of sequential system operation signals of said integrated circuit;

a plurality of probe lines coupled to said unit for carrying said system operation signals from predetermined probe points of said integrated circuit, wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said unit, said signal paths capable of moving said sets of sequential system operation signals at system operation clock rates;

a memory coupled to said unit and to said interface, said sets of sequential system operation signals stored in said memory at one or more clock signal rates internal to said integrated circuit and retrieved from said memory through said interface to said external process at one or more clock signal rates external to said integrated circuit so that said external diagnostics processor can process said captured system operation signals."

In rejecting claim 10, the Examiner stated:

"Whetsel teaches the invention substantially as claimed, including an integrated circuit [IC 10, Fig. 1] comprising:

"an interface [test port 38 of Fig. 2] for coupling to an external diagnostic processor;

"a unit [TCR control 26 of Fig. 2] responsive to instructions from said external diagnostic processor for capturing sets of sequential system operation signals of said integrated circuit;

"a memory [memory 30 of Fig. 2] coupled to said unit and to said interface, said sets of sequential system operations signals stored in said memory at one or more clock signal rates internal to said integrated circuit and retrieved from said memory through said interface to said external process at one or more clock signal rates external to said integrated circuit [test clock TCK of Fig. 1 and 2] so that said external diagnostic processor [external test bus controller 25 of Fig 1, col. 3 lines 35-63] can process said capture system operation signals.

"Whetsel teaches a plurality of lines [ODI of Fig. 1&2] coupled to said control unit for carrying said system operation signals from predetermined points [data bus 16 of Fig. 1] of said integrated circuit to said memory [DBM of Fig. 1], wherein said lines providing signal paths from said point to said memory, said signal path capable of moving sets of said system operation signals at system operation clock rates, said sets of system operation signal stored in said memory so that said sets of system operation signal are retrievable [see col. 4 lines 41-68 and claim 1]. However, Whetsel does not explicitly teach the plurality of probe lines comprises strings of storage elements for carrying said system operation signals.

"Gheewala teaches a cross-check test structure consists of a string of serial/parallel shift registers to control the probe lines and to observe the output of the sense lines [Fig. 4 and col. 8 lines 21-56].

> "It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the ODI of Whetsel to include the probe lines comprising a string of storage elements as taught by Gheewala for carrying data signals from the data bus to the memory. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so as a matter of design choice because it would enhance the test monitor operation to be controlled by the events detected over a range of DBM devices [see Whetsel col. 4 line 54 - col. 5 line 13]." Office Action, pages 5-6.

Again, even assuming *arguendo* that the combination of the Whetsel and the Gheewala '090 patents can be made, the combination simply does not teach nor suggest all the limitations of claim 10. Some of previous arguments made with respect to claim 1 are also applicable to claim 10, but claim 10 also provides additional limitations which are not met by the combination of references. The limitations of 1) an "integrated circuit;" 2) "probe lines...providing signal paths from said probe points to said unit;" 3) signal paths "capable of moving said sets of sequential system operation signals at system operation clock rates;" 4) a memory in which are stored sequential system operation signals at clock signal rates "internal to said integrated circuit;" and 5) system operation signals "retrieved from said memory through said interface" are not met by the combination, as argued below.

1. The Fundamental Misreading of Whetsel's Circuit Board System of Integrated Circuits and Applicants' "Integrated Circuit" is Repeated.

The Examiner repeats his misreading of Whetsel's circuit board system and applicants' claim of an integrated circuit in claim 10. The contradictory identifications of the integrated circuit IC1 10 as the applicants' "integrated circuit," and elements belonging to a second integrated circuit, DBM-1 20, as part of IC1-10 with claim 10 elements, "a unit responsive to ...", "a plurality of probe lines," and "a memory...", are maintained, as pointed out above. The applicants' additional "interface" element is also identified with IC1 10 and yet identified as test port 38, a part of second integrated circuit DBM-1 20, in another contradiction.

2. Even With the Misreading of the Whetsel Patent, the Cited References Do Not Teach the Limitation Wherein the "Probe Lines ...Comprise Strings of Storage Elements Providing Signal Paths from said Probe Points to Said Unit."

As in the case of claim 1, the Examiner identifies in applicants' claim 10, the "unit...for capturing sets of sequential system operation signals of said integrated circuit," as the Whetsel patent's TCR control 26 shown in Fig. 2 and the "probe lines," as Whetsel's ODI lines shown in Figs. 1 and 2. However, the probe line are described also as "comprising strings of storage elements providing signal paths from said probe points to said unit...". Setting aside the issue of the "strings of storage elements," purportedly met by combination with the Gheewala '090 patent, it should be evident from Fig. 6 of the Whetsel patent that the ODI lines do not provide signal paths from the bus to the TCR command [sic] register 26. Rather, "[t]he TCR control register 50 [sic] receives serial input on the TDI input and control input from the test port 38 via the L/S and DRCK 5 signals on the control bus 48." Col. 8, lines 58-61. Nowhere is there a mention of an input from the ODI lines.

3. The First Arrangement of the Combination of Whetsel and Gheewala '090 Patents Is Not "Capable of Moving Said Sets of Sequential System Operation Signals At System Operation Clock Rates."

Claim 10 further recites, "...said probe lines comprise strings of storage elements providing signal paths from said probe points to said unit, said signal paths capable of moving said sets of sequential system operation signals at system operation clock rates...." To meet the limitation of "strings of storage elements," the Examiner substituted or inserted the Gheewala serial/parallel shift registers for or into the ODI lines of Whetsel. As explained above, there are two possible arrangements for the serial/parallel shift registers in the Whetsel system. See pages 10-11 above.

In the first and most likely arrangement, Gheewala's serial/parallel shift register 28 is laid across the ODI lines of Whetsel to captures the bits from the ODI lines in parallel in one clock cycle and to serially move the captured bits out of the shift register in M clock cycles into the TCR 28 or memory 30. M = 16 in the Whetsel's specific embodiment. Where previously without the shift register 28, the Whetsel system could capture ODI data in one system clock cycle, the combined system must wait another 16 system clock cycles. However, claim 10 calls for the probe lines capable of moving said sets of "sequential" system operation signals at system operation clock rates. Such is not possible with the Gheewala's serial/parallel shift register 28. Any sequential

data on the buses 14 and 16 generated by the IC1 10 and IC2 12 within the 16-clock cycle waiting period is lost. The first arrangement cannot make the limitation.

Presumably the second arrangement of the combination of references can meet the limitation of "moving said sets of sequential system operation signals at system operation clock rates," albeit with a delay of N=16 clock cycles. In the second arrangement Gheewala's parallel/serial control shift register 27 is inserted into each of the ODI lines. However, the applicants again note that the dubiousness of the motivation to make the suggested combination and the added complexity of the combined system with an N-stage delay created by the Gheewala serial/parallel shift registers.

4. The Combination of Whetsel and Gheewala '090 Patents Does Not Store System Operation Signals At Clock Signal Rates "Internal to Said Integrated Circuit."

Claim 10 further requires "sets of sequential system operation signals stored in said memory at one or more clock signal rates internal to said integrated circuit" Nowhere in his rejection does the Examiner point out where signals at clock signal rates "internal to said integrated circuit," i.e., IC1 10, appear. The DBMs 20 and 22 are connected to a control bus 18 with clock signals (see Fig. 1) between the integrated circuits IC1 10 and IC2 12. It is self-evident that these clock signals are external to the integrated circuit IC1 10. Any clock signal on the bus 18 must travel through an input/output pin of the IC1 10 and cannot have a clock signal rate internal to the integrated circuit, a fact of integrated circuit design and which drives the applicants' claimed invention. See, for example, applicants' specification, page 1, lines 28-33 and page 3, lines 3-6.

5. The Combination of Whetsel and Gheewala '090 Patents Do Not Have System Operation Signals "Retrieved From Said Memory Through Said Interface."

Claim 10 also recites that the memory element which stores sets of sequential operation signals has these signals "retrieved from said memory through said interface...". The Examiner identified the applicants' interface as the "test port 38," shown in Fig. 2 of Whetsel. However, no data is retrieved from the memory 30 through the test port 38. Rather, data from the memory 30 is scanned out serially through the

TDO (Test Data Out) line which does not go through the test port 38. See Fig. 2 of Whetsel. Further details of the test port 38 illustrated in Fig. 3 and the text in col. 7, lines 49-60, show no connection to the TDO line. Hence this limitation is not met.

C. The Combination of Cited References Do Not Make The Limitations Of Method Claim 15.

Claim 15 recites:

"A method of operating an integrated circuit having logic blocks, a control unit, a memory and a plurality of probe lines of said logic blocks, said method comprising

operating said logic blocks to perform normal system operations at one or more system clock signal rates internal to said integrated circuit to produce sets of system operation signals;

enabling said probe lines responsive to said control unit to capture and carry said sets of system operation signals of said logic blocks at said system clock signal rates internal to said integrated circuit;

retrieving said sets of system operation signals from said logic blocks along said probe lines at said system clock signal rates internal to said integrated circuit,

storing said sets of system operation signals in said memory at said system clock signal rates internal to said integrated circuit; and

processing said sets of stored system operation signals to perform test and debug operations of said logic blocks of said integrated circuit."

In rationalizing his objection to claim 15, the Examiner stated:

"Whetsel teaches the invention substantially as claimed, including a method of operating an integrated circuit having logic blocks, a control unit, a memory and a plurality of lines of said logic blocks [see Fig. 1&2], said method comprising:

"operating said logic blocks to perform normal system operations [see claim 1] at one or more system clock signal rates internal to said integrated circuit to produce sets of system operation signals;

"enabling said lines [ODI lines, col. 4 lines 41-68] responsive to said control unit to capture and carry said sets of system operation signals of said logic blocks at said system clock signal rates internal to said integrated circuit;

"retrieving [col. 4 lines 41-68] said sets of system operation signals from said logic blocks along said lines at said system clock signal rates internal to said integrated circuit;

"storing [claim 1] said sets of system operation signals in said memory at said system clock signal rates internal to said integrated circuit; and

"processing [by external tester, col. 1 lines 30-57] said sets of stored system operation signals to perform test and debug operations of said logic block of said integrated circuit.

"Whetsel teaches a plurality of lines [ODI of Fig. 1&2] coupled to said control unit for carrying said system operation signals from predetermined points [data bus 16 of Fig. 1] of said integrated circuit to said memory [DBM of Fig. 1], wherein said lines providing signal paths from said point to said memory, said signal path capable of moving sets of said system operation signals at system operation clock rates, said sets of system operation signal stored in said memory so that said sets of system operation signal are retrievable [see col. 4 lines 41-68 and claim 1]. However, Whetsel does not explicitly teach the plurality of probe lines comprises strings of storage elements for carrying said system operation signals.

"Gheewala teaches a cross-check test structure consists of a string of serial/parallel shift registers to control the probe lines and to observe the output of the sense lines [Fig. 4 and col. 8 lines 21-56].

"It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the ODI of Whetsel to include the probe lines comprising a string of storage elements as taught by Gheewala for carrying data signals from the data bus to the memory. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so as a matter of design choice because it would enhance the test monitor operation to be controlled by the events detected over a range of DBM devices [see Whetsel col. 4 line 54 - col. 5 line 13]." Outstanding Office Action, pages 6-7.

Again according to the Examiner, the Whetsel patent teaches all the elements of the applicants' claim, except for the recited probe lines which are purportedly taught by the Gheewala '090 patent. But neither of the cited references teaches the applicants' limitations of 1) "a plurality of probe lines of said logic blocks;" 2) the step of "enabling said probe lines...to capture and carry said sets of system operation signals of said logic blocks at said system clock signal rates internal to said integrated circuit;" and 3) the step of "retrieving said sets of system operation said logic blocks along said probe lines at said system clock signal rates internal to said integrated circuit."

1. The Combination of Whetsel and Gheewala '090 Patents Does Not Have "A Plurality of Probe Lines of Said Logic Blocks".

Method claim 15 calls for the operation of "an integrated circuit having logic blocks, a control unit, a memory and a plurality of probe lines of said logic blocks..." and the step of "retrieving said sets of system operation signals from said logic blocks along said probe lines...". In his rejection of this claim, the Examiner did not explicitly identify the applicants' integrated circuit in the Whetsel patent so the applicants assume that IC1 10 in the Fig. 1 system is the intended analog from the rejection of device claims 1 and 10. The Examiner did repeat the identification of the applicants' probe lines as the Whetsel ODI lines in combination with serial/parallel shift registers of the Gheewala '090 patent.

Nowhere is there shown that IC1 10 has logic blocks, and perhaps more significantly, that ODI lines reach into IC1 10 so that there are "probe lines of said logic blocks." Rather, as described in col. 4, lines 19-21 and illustrated in Fig. 1 of the Whetsel patent, "[f]irst and second DBMs 20 and 22 are include in the circuit of FIG. 1 to provide for monitoring the signals on the data and address paths or leads between IC1 10 and IC2 12. The address and data bus signals to be monitored are input to the DBMs via ODI leads." The ODI lines merely monitor signals external to the IC1 10. Whether the bus signals are signals of logic blocks is unknown. This limitation is not met.

2. The Combination of Whetsel and Gheewala '090 Patents Does Not Capture and Carry System Operation Signals at System Clock Signal Rates "Internal to Said Integrated Circuit."

Claim 15 also recites the step of "enabling said probe lines...to capture and carry said sets of system operation signals of said logic blocks at said system clock signal rates internal to said integrated circuit." With the combination of references, the ODI lines must include the serial/parallel shift registers of the Gheewala '090 patent to perform the "capture and carry" operations.

However, as argued previously, nowhere is there shown in the Whetsel patent the use of any clock signals at "system clock signal rates internal to said integrated circuit," i.e., IC1 10. The only clock signals related to the integrated circuits, IC1 10 and IC2 12, are clock signals on the control bus 18 between the two integrated circuits on the system circuit board. See Fig. 1, and col. 3, lines 38-47. It should be evident that these

clocks signals are external to the integrated circuits, IC1 10 and IC2 12, not "internal to said integrated circuit."

3. The Combination of Whetsel and Gheewala '090 Patents Does Not Retrieve System Operation Signals at System Clock Signal Rates "Internal to Said Integrated Circuit."

Claim 15 further recites the step of "retrieving said sets of system operation from said logic blocks along said probe lines at said system clock signal rates internal to said integrated circuit". As argued immediately above, there is no teaching in the Whetsel patent of any clock running at a system operation rate internal to the integrated circuit IC1-10.

IV. SUMMARY AND CONCLUSION OF ARGUMENTS

From the arguments above, it should be evident that the Examiner has not met his burden of providing each and every requirement of MPEP §2143. The Examiner has not provided nor pointed out, a credible suggestion or motivation for combining the cited Whetsel and Gheewala '090 patents. The result of the combination of references is a poor and unsuccessful version of the Whetsel system. Finally, the references, either singly or in combination, neither teach nor even suggest all of the limitations in the applicants' claims. A *prima facie* case of obviousness to reject independent claims 1, 10 and 15 has not been made.

Hence claims 1, 10 and 15 are unobvious over the cited Whetsel and Gheewala '090 patents and should be allowed, along with claims 2-9, 11-14 and 16-22 dependent upon the independent claims. Therefore, the applicants respectfully request that the rejections be removed, all pending claims 1-22 be allowed, and the case passed to issue forthwith.

Respectfully submitted,

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Appendix

The following claims 1-22 as pending in this appeal. Representative independent claims 1, 10 and 15 argued in this appeal are marked in bold:

1. An integrated circuit having logic blocks comprising

a control unit for performing test and debug operations of said logic blocks of said integrated circuit;

a memory associated with said control unit, said memory holding instructions for said control unit; and

a plurality of probe lines responsive to said control unit for carrying system operation signals from predetermined probe points of said logic blocks, wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said memory, said signal paths capable of moving sets of said system operation signals at system operation clock rates, said sets of system operation signals stored in said memory so that said sets of system operation signals are retrievable.

2. The integrated circuit of claim 1 further comprising

a plurality of scan lines responsive to said control unit for loading test signals for said logic blocks and retrieving test signal results from said logic blocks, said test signals and said test signal results stored in said memory so that said loading and retrieving operations are performed at one or more clock signal rates internal to said integrated circuit.

3. The integrated circuit of claim 2 further comprising

a unit coupled to said control unit and said memory, said unit testing said logic blocks and said memory responsive to and in cooperation with said control unit to self-test said integrated circuit.

4. The integrated circuit of claim 2 wherein said scan lines comprise a first string of flip-flop connectors connected between a logic block and the remainder of said integrated circuit proximate said logic block, said flip-flop connectors providing signal paths between said logic block and the remainder of said integrated circuit proximate said logic block in one mode and carrying test signals and test signal results in a second mode.

5. The integrated circuit of claim 2 wherein said scan lines comprise a second string of flip-flop connectors between elements of a logic block, said flip-flop connectors providing signal paths between said logic block elements in one mode and carrying test signals and test signal results in a second mode.

6. The integrated circuit of claim 1 wherein each of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals at predetermined probe points of said logic blocks in one mode.

7. The integrated circuit of claim 6 wherein each programmable connector of said probe lines is programmed by a flip-flop connector, each flip-flop connector connected between elements of said integrated circuit and forming part of string of flip-flop connectors, said flip-flop connectors providing signal paths between said integrated circuit elements in one mode and carrying signals for programming said programmable connectors in a second mode.

8. The integrated circuit of claim 7 wherein at least some of said probe lines comprises a string of programmable connectors providing a signal path for carrying digital state system operation signals.

9. The integrated circuit of claim 7 wherein at least some of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals reflective of analog conditions at said predetermined probe points.

10. An integrated circuit comprising

an interface for coupling to an external diagnostic processor;

a unit responsive to instructions from said external diagnostic processor for capturing sets of sequential system operation signals of said integrated circuit;

a plurality of probe lines coupled to said unit for carrying said system operation signals from predetermined probe points of said integrated circuit, wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said unit, said signal paths capable of moving said sets of sequential system operation signals at system operation clock rates;

a memory coupled to said unit and to said interface, said sets of sequential system operation signals stored in said memory at one or more clock signal rates internal to said integrated circuit and retrieved from said memory through said interface to said external process at one or more clock signal rates external to said integrated circuit so that said external diagnostics processor can process said captured system operation signals.

11. The integrated circuit of claim 10 wherein said unit further comprises trigger logic responsive to said system operation signals for initiating storage of a set of said system operation signals in said memory.

12. The integrated circuit of claim 11 wherein said trigger logic is responsive to said system operation signals for terminating storage of said set of said system operation signals in said memory.

13. The integrated circuit of claim 10 wherein each of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals at predetermined probe points in one mode.

14. The integrated circuit of claim 13 wherein each programmable connector of said probe lines is programmed by a flip-flop connector, each flip-flop connector connected between elements of said integrated circuit and forming part of string of flip-flop connectors, said flip-flop connectors providing signal paths between said integrated circuit elements in one mode and carrying signals for programming said programmable connectors in a second mode.

15. A method of operating an integrated circuit having logic blocks, a control unit, a memory and a plurality of probe lines of said logic blocks, said method comprising

operating said logic blocks to perform normal system operations at one or more system clock signal rates internal to said integrated circuit to produce sets of system operation signals;

enabling said probe lines responsive to said control unit to capture and carry said sets of system operation signals of said logic blocks at said system clock signal rates internal to said integrated circuit;

retrieving said sets of system operation signals from said logic blocks along said probe lines at said system clock signal rates internal to said integrated circuit,

storing said sets of system operation signals in said memory at said system clock signal rates internal to said integrated circuit; and

processing said sets of stored system operation signals to perform test and debug operations of said logic blocks of said integrated circuit.

16. The method of claim 15 wherein said system operation signals comprise sequential system operation signals.

17. The method of claim 16 wherein said system operation signals comprise sets of sequential system operation signals.

18. The method of claim 15 wherein said integrated circuit has a plurality of scan lines of said logic blocks, said method further comprising

loading said memory with test signals and instructions for said control unit;

loading said scan lines responsive to said control unit with said test signals for said logic blocks at one or more clock signal rates internal to said integrated circuit;

operating said logic blocks at one or more clock signal rates internal to said integrated circuit;

retrieving test signal results from said logic blocks along said scan lines at one or more clock signal rates internal to said integrated circuit,

storing said test signal results in said memory at one or more clock signal rates internal to said integrated circuit; and

processing said stored test results signals in said control unit responsive to said stored instructions in said memory to perform test and debug operations of said logic blocks of said integrated circuit.

19. The integrated circuit of claim 10 wherein said memory is also coupled to said system operation unit so that said memory unit may be accessed selectively or simultaneously by said data capture unit and said system operation unit.

20. The method of claim 1 wherein said system operation signals comprise sequential system operation signals.

21. The method of claim 20 wherein said system operation signals comprise sets of sequential system operation signals.

22. The method of claim 1 wherein said system operation signals are stored in said memory at one or more clock signal rates internal to said integrated circuit.